Amendments to the Claims (this listing replaces all prior versions):

1. (currently amended) A method comprising:

from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format, determining a type; and

writing an entry to a memory management table specifying one of the at least two types of endian conversion based on the determining.

2. (previously presented) The method of claim 1 wherein writing an entry to a memory management table further includes specifying the location of the portion of data within the memory system.

3. (previously presented) The method of claim 1 wherein the at least two types of endian conversion include a data coherent conversion.

4. (previously presented) The method of claim 1 wherein the at least two types of endian conversion include an address coherent conversion.

5. (previously presented) The method of claim 1 wherein the entry includes a single bit for specifying one of two types of endian conversion.

6. (previously presented) The method of claim 1 wherein the entry maps a virtual memory address to a physical memory address.

7. (currently amended) A method comprising:

maintaining a memory management table that includes one or more entries, each entry defining a location of a portion of data stored within a memory system and ~~indicating~~ specifying

a type determined from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format.

8. (previously presented) The method of claim 7 wherein the at least two types of endian conversion include a data coherent conversion.

9. (previously presented) The method of claim 7 wherein the at least two types of endian conversion include an address coherent conversion.

10. (previously presented) The method of claim 7 wherein the entry includes a single bit for specifying one of the at least two types of endian conversion.

11. (original) The method of claim 7 wherein the portion of data is stored at a physical memory address within a memory system.

12. (previously presented) The method of claim 11 wherein the entry maps the physical address at which the portion of data is stored to a virtual address accessible by a processor.

13. (currently amended) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format, determine a type; and

write an entry to a memory management table specifying one of the at least two types of endian conversion based on the determining.

14. (previously presented) The computer program product of claim 13 wherein the at least two types of endian conversion include a data coherent conversion.

15. (previously presented) The computer program product of claim 13 wherein the at least two types of endian conversion include an address coherent conversion.

16. (previously presented) The computer program product of claim 13 wherein the entry includes a single bit for specifying one of two types of endian conversion.

17. (previously presented) The computer program product of claim 13 wherein the entry maps a virtual memory address to a physical memory address.

18. (currently amended) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

maintain a memory management table that includes one or more entries each entry defining a location of a portion of data stored within a memory system and ~~indicating~~ specifying a type determined from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format.

19. (previously presented) The computer program product of claim 18 wherein the at least two types of endian conversion include a data coherent conversion.

20. (previously presented) The computer program product of claim 18 wherein the at least two types of endian conversion include an address coherent conversion.

21. (previously presented) The computer program product of claim 18 wherein the entry includes a single bit for specifying one of the at least two types of endian conversion.

22. (original) The computer program product of claim 18 wherein the portion of data is stored at a physical memory address within a memory system.

23. (previously presented) The computer program product of claim 22 wherein the entry maps the physical address at which the portion of data is stored to a virtual address accessible by a processor.

24. (previously presented) A memory management table residing in computer memory comprising:

one or more table entries, with each table entry having a first field for defining the location of a portion of data stored within a memory system and a second field for defining a type determined from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format.

25. (previously presented) The memory management table of claim 24 wherein each entry includes a single bit for specifying one of the at least two types of endian conversion.

26. (previously presented) The memory management table of claim 24 wherein the at least two types of endian conversion include a data coherent conversion.

27. (previously presented) The memory management table of claim 24 wherein the at least two types of endian conversion include an address coherent conversion.

28. (previously presented) The memory management table of claim 24 wherein each entry maps a virtual memory address to a physical memory address.

29. (currently amended) A system comprising:

a first processor for processing data in a first endian format;

a second processor for processing data in a second endian format;

a bus for interconnecting the first and second processors;

an endian converter for converting portions of data from the first endian format to the second endian format; and

a memory management table including one or more entries, with each entry defining a location for a portion of data stored within a memory system to be converted from the first endian format to the second endian format, and ~~indicating~~ specifying a type determined from at least two types of endian conversion, including a first type to convert data from the first endian format to the second endian format and a second type to convert data from the first endian format to the second endian format.

30. (previously presented) The system of claim 29 wherein the at least two types of endian conversion include a data coherent conversion.

31. (previously presented) The system of claim 29 wherein the at least two types of endian conversion include an address coherent conversion.

32. (original) The system of claim 29 wherein the first processor is a little-endian processor.

33. (original) The system of claim 29 wherein the second processor is a big-endian processor.

34. (currently amended) A computer architecture comprising:

a networking device, including:

a first processor for processing data in a first endian format;

a second processor for processing data in a second endian format;

a bus for interconnecting the first and second processors;

an endian converter for converting portions of data from the first endian format to the second endian format; and

a memory management table including one or more entries, with each entry defining a location for a portion of data stored within a memory system to be converted from the first endian format to the second endian format, and ~~indicating~~ specifying a type determined from at least two types of endian conversion, including a first type to convert data from the first endian format to the second endian format and a second type to convert data from the first endian format to the second endian format.

35. (previously presented) The architecture of claim 34 wherein the at least two types of endian conversion include a data coherent conversion.

36. (previously presented) The architecture of claim 34 wherein the at least two types of endian conversion include an address coherent conversion.

37. (original) The architecture of claim 34 wherein the first processor is a little-endian processor.

38. (original) The architecture of claim 34 wherein the second processor is a big-endian processor.

39. (previously presented) A method comprising:

accessing a table entry of a memory management table, wherein the table entry is associated with a portion of data stored within a memory system and includes a conversion-type indicator; and

from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format determining a type based on the conversion-type indicator.

40. (previously presented) The method of claim 39 wherein the at least two types of endian conversion include a data coherent conversion.

41. (previously presented) The method of claim 39 wherein the at least two types of endian conversion include an address coherent conversion.

42. (original) The method of claim 39 wherein the conversion-type indicator includes a single bit for specifying one of the at least two types of endian conversion.

43. (previously presented) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

access a table entry of a memory management table, wherein the table entry is associated with a portion of data stored within a memory system and includes a conversion-type indicator; and

from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format, determine a type based on the conversion-type indicator.

44. (previously presented) The computer program product of claim 43 wherein the at least two types of endian conversion include a data coherent conversion.

45. (previously presented) The computer program product of claim 43 wherein the at least two types of endian conversion include an address coherent conversion.

46. (previously presented) The computer program product of claim 43 wherein the conversion-type indicator includes a single bit for specifying one of the at least two types of endian conversion.

47. (currently amended) A method comprising:

from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first endian format, determining a type; and

writing an entry to a memory management table specifying one of the at least two types of endian conversion based on the determining.

48. (previously presented) The method of claim 47 wherein writing an entry to a memory management table further includes specifying the location of the portion of the page within the memory system.

49. (previously presented) The method of claim 47 wherein the at least two types of endian conversion include a data coherent conversion.

50. (previously presented) The method of claim 47 wherein the at least two types of endian conversion include an address coherent conversion.

51. (previously presented) The method of claim 47 wherein the first type is a data coherent conversion and the second type is an address coherent conversion.

52. (previously presented) The method of claim 1 wherein the first endian format is big endian.

53. (previously presented) The method of claim 1 wherein the first endian format is little endian.